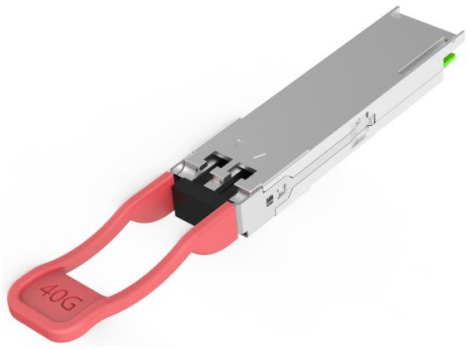
40Gb/s QSFP+ 40km Transceiver

Features

- Up to 11.2Gb/s data rate per channel
- 4 CWDM lanes MUX/DEMUX
- Up to 40km transmission
- SMF LC duplex connector
- QSFP+ MSA compliant
- Electrically hot-pluggable
- Optical link budget: 16dBm
- RoHS-6 compliant and lead-free
- Support Digital Monitoring interface
- Single +3.3V power supply
- Maximum power consumption 3.5W
- All-metal housing for superior EMI performance
- Case operating temperature
  Commercial: 0 ~ +70ºC
  Extended: -10 ~ +80ºC
  Industrial: -40 ~ +85ºC



Applications

- 40G Ethernet
- Data Center
- Back to Back
- InfiniBand QDR

Part Number Ordering Information

Part Number	Data Rate (Gb/s)	Wavelength (nm)	Transmission Distance(km)	Temperature (ºC) (Operating Case)
FBL3-ER041C	40	1271/1291/ 1311/1331	40	0~70 commercial
FBL3-ER041E	40		40	-10~80 Extended
FBL3-ER041I	40		40	-40~85 Industrial

I. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	85	°C	
Power Supply Voltage	V_{CC}	0	3.47	V	
Relative Humidity (non-condensation)	RH	5	95	%	
Damage Threshold	TH_d	0		dBm	

II. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	T_{OP}	0		70	°C	commercial
		-40		85	°C	Industrial
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate			40		Gb/s	
Control Input Voltage High		2		Vcc	V	
Control Input Voltage Low		0		0.8	V	
Link Distance (SMF)	D			40	km	9/125um

III. General Description

FB-LINK'FBL3-ER041C is a parallel 40Gb/s Quad Small Form-factor Pluggable (QSFP+) optical module and designed for 40km optical communication applications. The module converts 4 inputs channels (ch) of 10Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

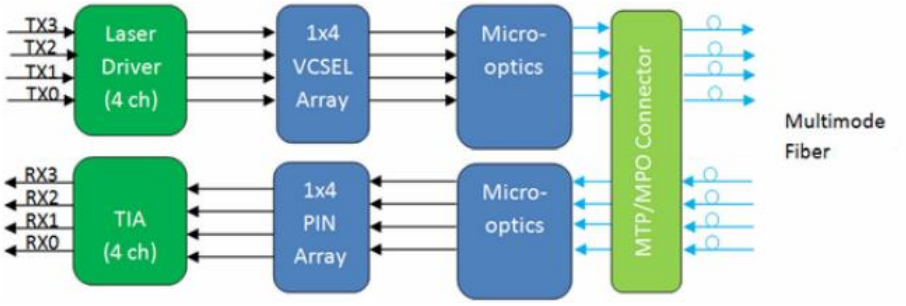
The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module.

The module operates by a single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet

the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

IV. Transceiver Block Diagram



V. Pin Assignment and Pin Description

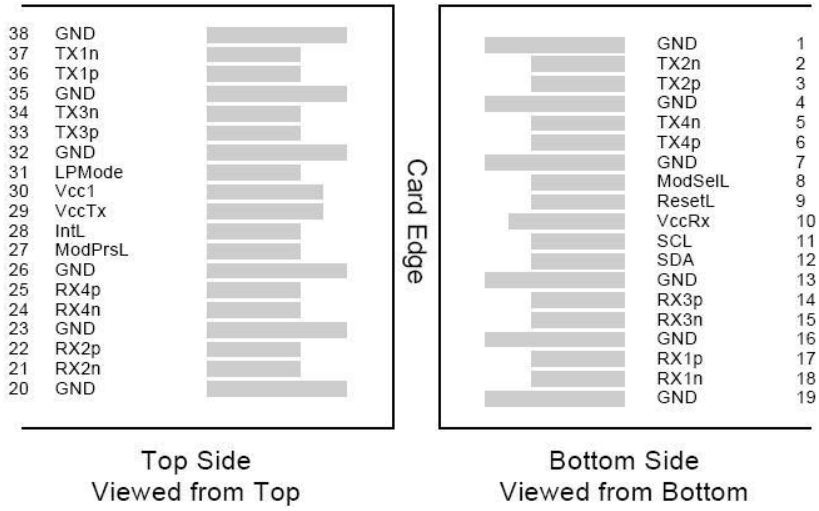


Figure1. QSFP+ Transceiver Electrical Pad Layout

PIN	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1

8	LVTLL-I	ModSelL	Module Select	3
9	LVTLL-I	ResetL	Module Reset	4
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	5
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	5
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	6
28	LVTTL-O	IntL	Interrupt	7
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMode	Low Power Mode	8
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	

37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP+ modules. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 4 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.
3. Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP+ module must be used.
4. The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.
5. Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.
6. Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state.
7. Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board
8. Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

VI. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max	Unit	Notes
Power Consumption	p			3.5	W	
Supply Current	Icc			900	mA	

Transmitter						
Single-ended Input Voltage Tolerance	Vcc	-0.3		4.0	V	
Differential Input Voltage Swing	Vin,pp	190		700	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Transmit Disable Assert Time				10	us	
Transmit Disable Voltage	Vdis	Vcc-1.3		Vcc	V	
Transmit Enable Voltage	Ven	Vee		Vee +0.8	V	
Receiver						
Single-ended Input Voltage Tolerance	Vcc	-0.3		4.0	V	
Differential Output Voltage Swing	Vout,pp	300		850	mVpp	
Differential Output Impedance	Zout	90	100	110	Ohm	
J9 Jitter Output	Jo9			0.65	UI	
LOS Assert Voltage	VlosH	Vcc-1.3		Vcc	V	
LOS De-assert Voltage	VlosL	Vee		Vee +0.8	V	

VII. Optical Characteristics

The following optical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Transmitter						
Lane wavelength（range）	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	

Spectral Band Width	λ			1	nm	
Signaling rate, each lane			11.2		GBd	
Side-mode suppression ratio	SMSR	30				
Total launch power				8.3	dBm	1
Average launch power, each lane	Pavg	-2.7		4.5	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter and Dispersion Penalty, each lane	TDP			2.3	dB	
OMA minus TDP, each lane	OMA-TDP	-2.3			dBm	
Average launch power of OFF transmitter, each lane		Poff		-30	dBm	
Transmitter reflectance				-12	dB	
Transmitter eye mask {X1, X2,X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Receiver						
Signaling rate, each lane			11.2		GBd	
Receiver Sensitivity (Average Power), each Lane	Sen.			-19	dBm	2
Input Saturation Power (Overload)	Psat	3.3			dBm	
Receiver reflectance	Rr			-26	dB	
LOS Assert	Plos_on	-35			dBm	
LOS De-assert	Plos_off			-23		
LOS Hysteresis		0.5		4	dB	

Notes:

1. Class 1 Laser Safety per FDA/CDRH and IEC-825-1 regulations.
2. Measured with Light source 1271/1291/1311/1311nm, ER=3.5dB; BER≤1E-12 @40Gbps, PRBS=2^{31} -1 NRZ.

VIII. Digital Diagnostic Functions

The following digital diagnostic characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min.	Max	Unit	Notes
Temperature monitor absolute error	DMI_ Temp	-3	3	ºC	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-0.15	0.15	V	Full operating range
RX power monitor absolute error	DMI_RX	-3	3	dB	
Bias current monitor	DMI_ bias	-10%	10%	mA	
TX power monitor absolute error	DMI_TX	-3	3	dB	

IX. Mechanical Dimensions

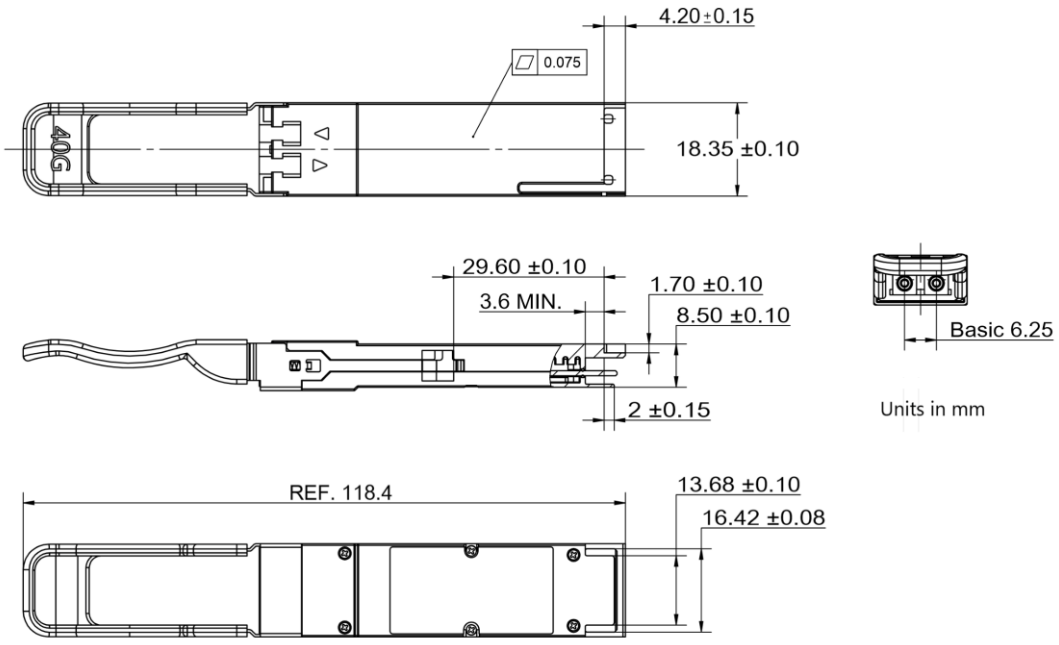


Figure2. Mechanical Outline

X. Revision History

Version No.	Initiated	Revised contents	Release Date
V1.0	Andy Zhang	Preliminary datasheet	2018-09-20